



RoodMicrotec Newsletter

August 2010 • RoodMicrotec

‘The Semiconductor Industry Association (SIA) reports exceptionally robust sales in the first half of 2010. Worldwide semiconductor sales were more than 50 percent up from the same period of 2009 when sales totalled \$96.1 billion. The Association expects that sequential growth rates will moderate in the next few months, bringing year-on-year growth in the industry in line with its mid-year forecast of 28.4 percent.

‘RoodMicrotec also anticipates a slightly more modest, but still significant growth in the second half of the year. As stated in our press release of 6 July, we have been realising sales growth for several successive quarters. We are clearly on the right track,’ said RoodMicrotec CEO Philip Nijenhuis.

‘This is also borne out by the seminar we are organising on 21 October, to which we cordially invite you in this newsletter. A number of well-known industry experts will speak, and there will be a presentation from Landis

& Gyr, a major fabless company. Landis & Gyr is ideally placed to explain their experiences and how RoodMicrotec meets their needs.

I am looking forward to seeing you on 21 October.’

Agenda

Preliminary announcement:

October 21, 2010, 9 am to 5 pm

RoodMicrotec conference: Solutions for reliable, timely and cost-effective results aimed at Fabless Design Companies, Nördlingen, Germany.

Next to the lectures, plant tours are offered. In addition, ATE equipment from 3 suppliers will be displayed in a showroom. More details will follow at a later date.

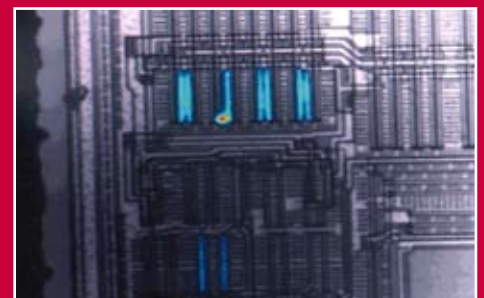
Failure Analysis is a step by step process

‘We use different tools and techniques to locate a failure in a device’, says Friedrich Dreher of RoodMicrotec’s Failure & Technology business unit.

‘The process of determining how or why a semiconductor device has failed is often done step by step. Device failure is defined as any non-conformance of the device to its electrical and/or visual/mechanical specifications. For example, when we perform an electrical measurement we might find a current that is much too high, which is an indication of a defect. Such a failure may be present even if the device is still functional. Obviously, non-destructive FA techniques are done before destructive ones. It is also important to solve any inconsistencies in the results before proceeding to the next step.

The results of the various failure analysis techniques will eventually point to the real failure. The most commonly used technique is Photo Emission Microscopy (PEM). PEM utilises local variations in electron emission to generate image contrast. The excitation is usually produced by UV light. In our specific case, defects in semiconductors tend to emit light where there is a defect.

An older, but still used technique, is the liquid crystal technique. Liquid crystal is used to locate areas on the die surface that exhibit excessive heating. As a leakage tends to have a higher temperature, this is a way to detect a defect.’



RoodMicrotec offers tailored approach

Counterfeit products are risky

'It has always been attractive to fake quality products, in particular expensive ones, to make quick money. Especially after a crisis the number of fake products on the market tends to grow drastically,' says Arno Rudolph, sales & marketing manager at RoodMicrotec. 'This is indeed what happened after the most recent crisis. During the crisis customers for electronic components cleared their stocks

and manufacturers received fewer or no orders for such components.

Now that the crisis has gradually been overcome, there is suddenly so much demand for components that manufacturers cannot cope.

As a result, resellers like distributors, dealers and chip brokers, but also the buying departments of system level manufacturers are

looking for alternative channels, mainly in the Far East. Unfortunately some of these sources are unknown, which increases the risk of parts being counterfeit. Reselling such parts to end-customers is very risky (see below). This not just endangers the vendor-customer relationship – if the case becomes public, the vendor's reputation may be seriously affected.'

RISK	EFFECT
No chip (die) in package	Device does not work
Cloned die in package (not original)	Device works, but not the same quality/lifetime...
Faked die in package (totally different from original)	Device works differently
'Dead' die in package (totally failed original part)	Looks original, but does not work
Failed die in package (e.g.: failed at high temperature)	Looks original, works, but not in specified temp range
Device is over-age (stored too long)	Chip delaminations, solder ability problems (oxide), popcorn effect when soldering due to moisture in plastic packages...

RoodMicrotec's solution

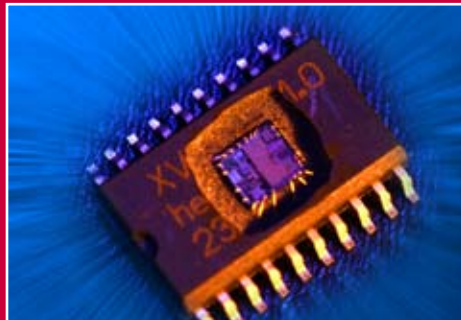
'Specialists like RoodMicrotec can offer their services here, equipped as we are with measurement devices and vast knowledge in this field. We have developed a brochure that explains our working methods detailing the different steps and the required time, costs and what specific tests do and do not determine (see attachment). All steps can be combined according to our customer's requirements. Our systematic approach allows for

checks to be made to exclude as many residual risks as the customer requires. The time frame for the activities varies from 24 hours to several weeks, and the costs from about 100€ to several 10k€.

RoodMicrotec's approach shows customers clearly what they can expect for their money, and it is up to the customer to select an optimum cost/time/remaining risk balance for each individual case.'



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Invitation

Einladung

Uitnodiging



RoodMicrotec Seminar

Solutions for reliable, timely and cost-effective results aimed at Fabless Design Companies

An ongoing trend in the semiconductor industry is to use different partners for individual process steps such as design, wafer manufacturing, wafer probing, assembly and final test.

The key challenge is to meet all quality and reliability requirements throughout the entire process. The growing requirements in the industry such as 'zero defect', in-time development and delivery, or cost pressure from the market are focus of this RoodMicrotec seminar organised by well-known industry experts.

- Helmut Keller, Chairman Europe SAE, Automotive Electronics Reliability Committee
(**Reliable products through 'Robustness Validation'**: an advanced qualification methodology to validate the robustness of semiconductors)
- Prof. Peter Jacob, Scientist at EMPA Switzerland
(**In-time development by 'FIB' chip modification**: how to use FIB services)
- Prof. Vierhaus, Head of Chair 'technical informatic' at Technical University Cottbus, Germany
(**Cost-effectiveness by 'design-for-test'**: how to design for testability)

Presentations on safe launch methodology, printed circuit board qualification and selection of economic test platforms will complement the programme.

Attend our seminar to learn more about these important topics!

Automatic Test Equipment (ATE) will be demonstrated in a showroom and plant tours are offered all day.

Key info:	Date	October 21, 2010 - Thursday
	Time	9:00 am – 5:30 pm
	Location	RoodMicrotec in Nördlingen, Germany
	Language	English

Aimed at:

Decision-makers from Fabless Design Companies and from design departments of OEM Companies
Semiconductor professionals like product engineers, quality engineers and test engineers

Programme details, registration procedure, etc. to be confirmed.

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